REMARKS

Claims 14-24 are currently pending in the application. By this response, no claims are amended, added, or canceled. Reconsideration of the rejected claims in view of the following remarks is respectfully requested.

35 U.S.C. §103 Rejection

Claims 14-20 were rejected under 35 U.S.C. §103(a) for being unpatentable over U.S. Patent Application Publication No. 2004/0144979 issued to Bhattacharyya ("Bhattacharyya")[1] in view of U.S. Patent No. 5,384,473 to Yoshikawa et al. ("Yoshikawa"). This rejection is respectfully traversed.

The Examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP §2142.

The invention relates to stacked circuits, and more particularly to stacked circuits having different crystal orientations. In non-limiting exemplary embodiments of the invention, a first CMOS device, such as a pFET, is formed having a first crystal orientation in the active region of the device, and a second CMOS device, such as an nFET, is formed having a second orientation in the active region of the second device.

[1] Applicants note that the application upon which U.S. Patent Application Publication No. 2004/0144979 is based has issued to U.S. Pat. No. 6,808,971.

After both devices are formed, the second device is bonded to the first device with a bonding layer forming a stacked or layered arrangement. Once the two devices are bonded in the stacked arrangement, the devices are interconnected with conductive pathways. Thus, it is possible to form stacked layers of CMOS devices where each layer has either the same or a different crystal orientation in the active region as a layer below it and/or a layer above it. Advantages of the multilayer SOI device include a reduction of about 50% of the area needed to create a circuit, such as, for example, a CMOS inverter. Claim 14 recites, in part

> ... a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation; and
>
> an upper semiconductor device having an active region comprising a semiconductor with a second crystal orientation, wherein the upper semiconductor device is formed separately from the lower semiconductor device and connected thereto by an interconnect structure.

The Examiner asserts that Bhattacharyya discloses a lower device in FIG. 9, an upper semiconductor device in FIG. 10, and that the two devices are shown connected in FIG. 11. The Examiner admits that Bhattacharyya does not disclose first and second crystal orientations. The Examiner asserts that Yoshikawa teaches first and second crystal orientations, and that it would have been obvious to combine the teachings of Bhattacharyya and Yoshikawa. Applicants respectfully disagree.

Bhattacharyya discloses a CMOS inverter and method of making the same. In FIGS. 2-7, Bhattacharyya shows and describes a method of making a single device (either NFET or PFET). FIGS. 8-9 show the fabrication of an NFET device subsequent to the intermediate structure shown in FIG. 7. Alternatively, FIG. 10 shows the

fabrication of a PFET device subsequent to the intermediate structure shown in FIG. 7. FIG. 11 shows a CMOS inverter that utilizes either the NFET of FIG. 9, or the PFET of FIG. 10, but not both. That is, contrary to the Examiner's assertion, the CMOS inverter 100 shown in FIG. 11 includes the NFET device of FIG. 9, but does not include the PFET of FIG. 10. This is evidenced by the fact that the lower device in FIG. 11 comprises layer 110, but does not comprise layer 26. Layer 110 is necessarily different from layer 26, because the reference number is different and Bhattacharyya explicitly states that the numbering used in FIG. 11 will be identical to that used in FIGS. 8 and 10 where appropriate. Thus, contrary to the Examiner's opinion in the outstanding Office Action, Bhattacharyya's CMOS inverter 100 shown in FIG. 11 does not comprise the device of FIG. 9 and the device of FIG. 10 formed separately and connected by an interconnect structure.

Therefore, Applicants submit that the Examiner is improperly picking and choosing elements from different embodiments of Bhattacharyya in an attempt to arrive at the claimed invention. Such piece-meal reconstruction of the claimed invention is improper, and the rejection should be withdrawn for at least this reason.

In any event, Applicants submit that the CMOS inverter 100 depicted in FIG. 11 does not comprise a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation, as recited in claim 14. In fact, there is no teaching or suggestion that the semiconductor material 110 is crystallized or comprises a crystal orientation.

Yoshikawa does not compensate for the deficiencies of Bhattacharyya with respect to claim 14. Instead, Yoshikawa discloses a semiconductor body 20 comprising

a first semiconductor substrate 10 laminated to a second semiconductor substrate 12 (FIG. 1B). NMOS 26 and PMOS 28 are formed on portions of the semiconductor body 20. Applicants acknowledge that Yoshikawa discloses a first substrate portion having a first surface orientation of [100] and a second substrate portion having a second surface orientation of [110]. However, Yoshikawa teaches these first and second portions having different crystal orientations are formed on the same device (e.g., FIG. 1F), not in an upper device and a lower device, as recited in claim 14. Therefore, combining the teachings of Yoshikawa and Bhattacharyya would not result in the claimed invention, but, rather, would result in Bhattacharyya's layer 26 of upper device 50 in FIG. 11 having Yoshikawa first and second portions having different crystal orientations. However, such a structure does not comprise a lower semiconductor device having an active region comprising a semiconductor with a first crystal orientation, as recited in claim 14. Therefore, the applied references do not teach or suggest each and every feature of the claimed invention.

Moreover, Applicants respectfully submit that the combination of Bhattacharyya and Yoshikawa is improper because Yoshikawa is non-analogous art. Bhattacharyya is directed to CMOS constructions comprising semiconductor-on-insulator (SOI) technology. Bhattacharyya teaches in the Background section that:

> SOI technology differs from traditional bulk semiconductor technologies in that the active semiconductor material of SOI technologies is typically much thinner than that utilized in bulk technologies. The active semiconductor material of SOI technologies will typically be formed as a thin film over an insulating material (typically oxide), with exemplary thicknesses of the semiconductor film being less than or equal to 2000 Å. In contrast, bulk semiconductor material will typically have a thickness of at least about 200 microns. The thin semiconductor of SOI technology can allow higher

> performance and lower power consumption to be achieved in integrated circuits than can be achieved with similar circuits utilizing bulk materials. (Bhattacharyya, paragraph 0002).

Yoshikawa, on the other hand, is not directed to SOI technology. Yoshikawa clearly does not teach or suggest SOI technology in which a thin film of semiconductor material is formed over an insulator that is, in turn, formed over a substrate. In fact, Yoshikawa is directed to the traditional bulk semiconductor technologies that Bhattacharyya distinguishes from SOI technology in the above-noted passage. The skilled artisan concerned with SOI structure and fabrication techniques would not look to traditional bulk semiconductor technologies for guidance. Thus, Yoshikawa is non-analogous art and there is no motivation to combine Bhattacharyya and Yoshikawa.

Claims 15-20 are dependent claims, depending from a distinguishable independent claim. Accordingly, claims 15-20 are also distinguishable and are in condition from allowance for at least the reasons discussed above.

Accordingly, Applicants respectfully request that the rejection over claims 14-20 be withdrawn.

Other Matters

Applicants note that the Examiner did not include claims 21-24 in the above noted rejection under §103. Moreover, the Examiner did not assert any other rejection or objection regarding these claims. However, the Examiner failed to indicate that these claims are allowable, and asserted on the Office Action Summary (PTOL-326) dated July 25, 2006 that claims 14-24 are rejected. Because no rejections or objections have

been applied to claims 21-24, these claims should be indicated allowable. Moreover, Applicants respectfully submit that if the Examiner subsequently rejects claims 21-24 in the next Official Action, that action cannot properly be made final pursuant to MPEP 706.07(a).

CONCLUSION

In view of the foregoing remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicant hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,
Mahmoud A. Mousa

Andrew M. Calderon
Reg. No. 38,093

October 20, 2006
GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191